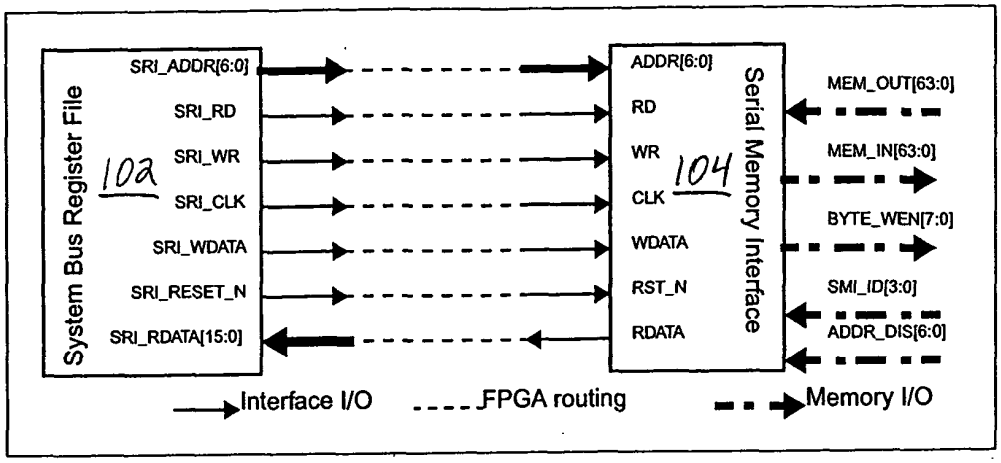
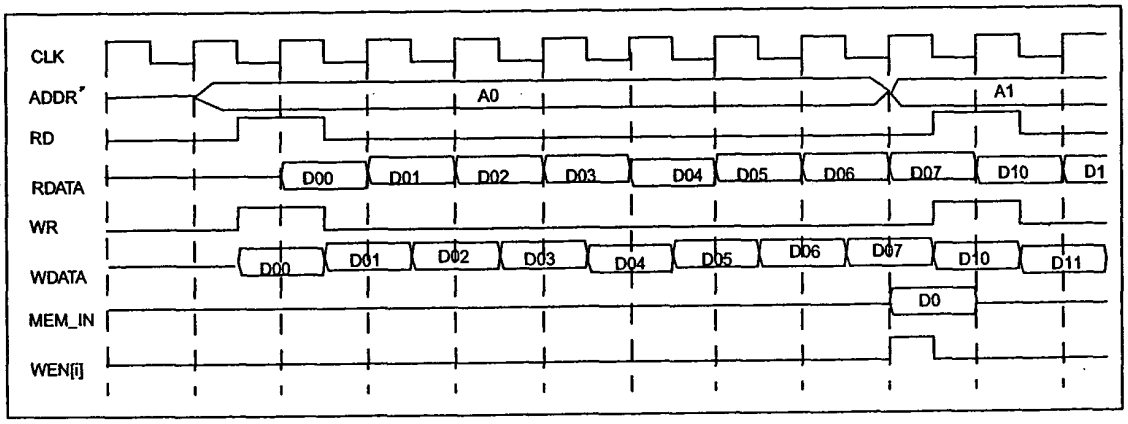


100

Fig. 1



200

Fig. 2

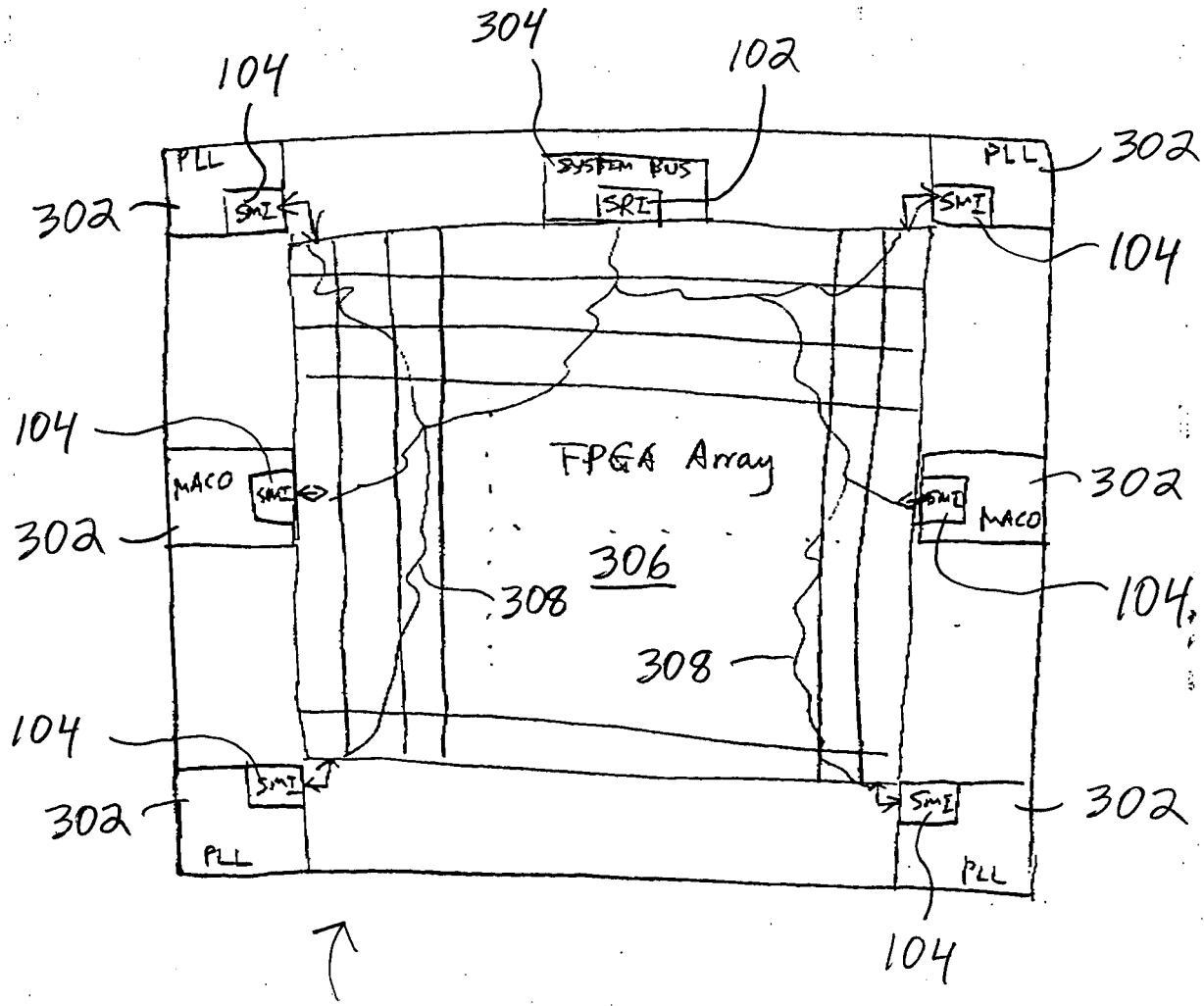
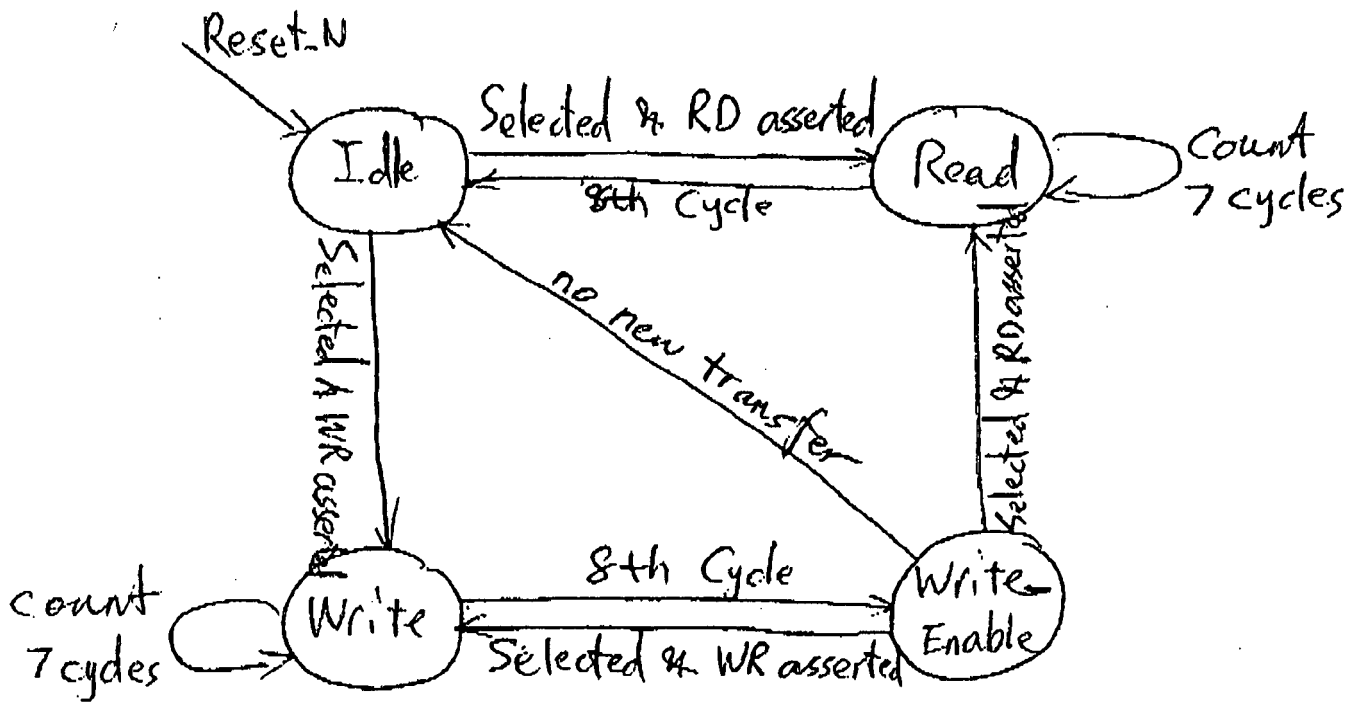

304
102
104
PLL
SYSTEM BUS
SRI
PLL
302
302
SMI
SMI
104
104
FPGA Array
MACO
SMI
SMI
MACO
302
302
306
308
104
308
104
SMI
SMI
302
302
PLL
PLL
104
300

Fig. 3



* Selected = ADDR matches ID
* In Write_Enable state, WEN asserted

Fig. 4

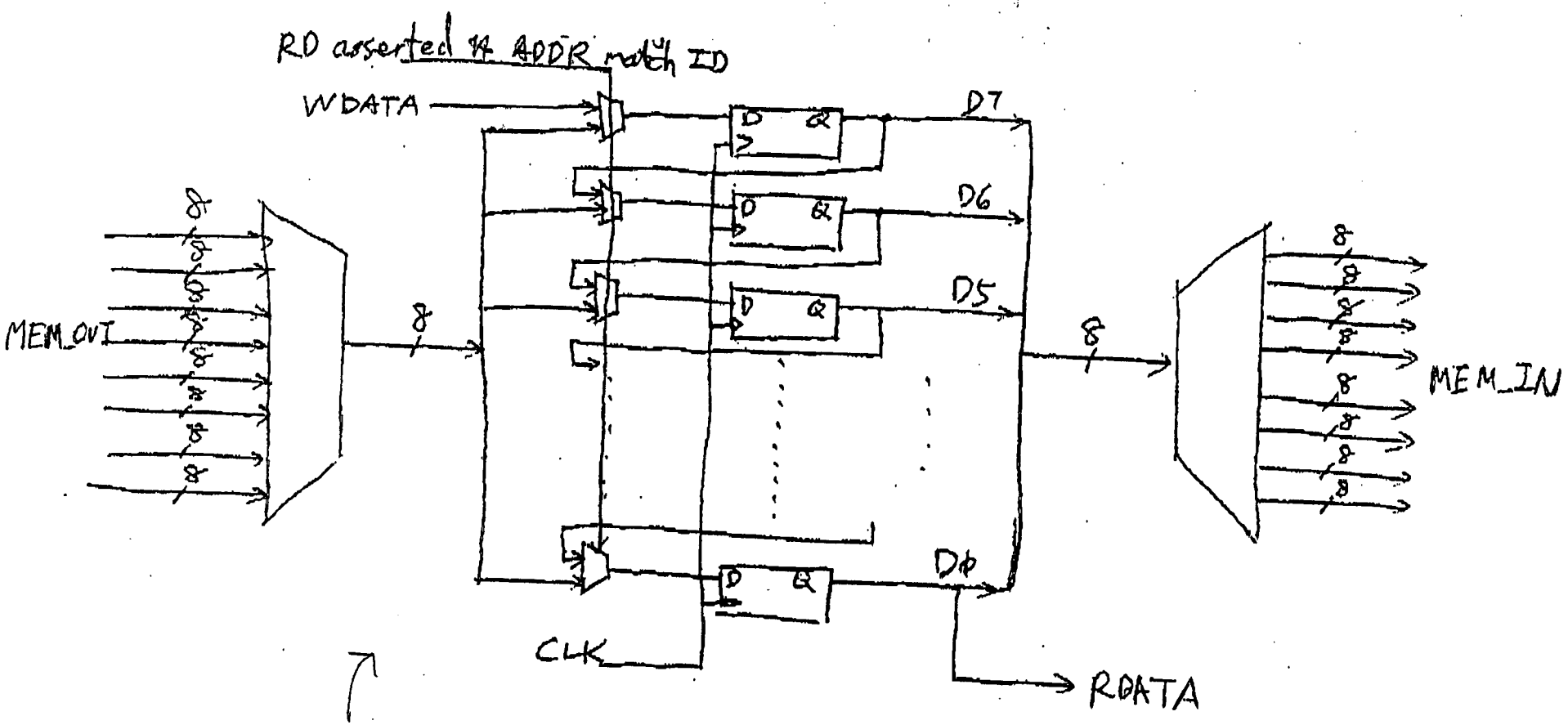

RD asserted & ADDR match ID
WDATA
MEM_OUT
8
D
Q
D7
D6
D5
D0
CLK
RDATA
MEM_IN
500

Fig. 5